Claims

What is claimed is:

1. A circuit for reducing propagation delay, comprising:

a logic circuit including a p-type transistor and an n-type transistor, wherein a drain of the p-type transistor is coupled to a drain of the n-type transistor; and

a voltage offset circuit that is arranged to provide a first voltage to a gate of the p-type transistor, and further arranged to provide a second voltage to a gate of the n-type transistor such that the second voltage is positively offset relative to the first voltage.

2. The circuit of Claim 1, wherein the logic circuit is arranged as an inverter circuit.

3. The circuit of Claim 1, wherein the voltage offset circuit includes a resistor circuit.

4 The circuit of Claim 3, wherein the resistor circuit includes a plurality of resistive elements that are configured in at least one of a series and a parallel arrangement.

5. The circuit of Claim 1, wherein the voltage offset circuit includes a capacitor circuit.

6 The circuit of Claim 5, wherein the capacitor circuit includes a plurality of capacitive elements that are configured in at least one of a series and a parallel arrangement.

7. The circuit of Claim 5, wherein the capacitive circuit enables an effective supply voltage that is greater than a relatively smaller supply voltage.

8. The circuit of Claim 7, wherein the effective supply voltage enables at least part of a reduction in a propagation delay associated the relatively smaller supply voltage.

9. The circuit of Claim 1, further comprising a current source circuit that is configured to provide a current.

10. The circuit of Claim 1, wherein the first voltage operates as a ramp and the second voltage operates as a relatively different ramp.

11. A timer circuit for reducing propagation delay for a relatively small supply voltage, comprising:

a current source circuit that is configured to provide a current;

a capacitor circuit that is configured to provide a first voltage in response to the current;

a voltage offset circuit that is coupled between the current source circuit and the capacitor circuit, wherein the voltage offset circuit is arranged to provide a second voltage in response to the first voltage and the current such that the second voltage is positively offset relative to the first voltage; and

an inverter circuit that includes a p-type transistor and an n-type transistor, wherein a drain of the p-type transistor is coupled to a drain of the n-type transistor, a gate of the p-type resistor is arranged to receive the first voltage, and a gate of the n-type resistor is arranged to receive the second voltage.

12 The circuit of Claim 11, wherein the voltage offset circuit includes a resistor circuit.

13. The circuit of Claim 11, wherein the voltage offset circuit includes a capacitor circuit.

14. The circuit of Claim 13, wherein the capacitive circuit enables an effective supply voltage that is greater than a relatively smaller supply voltage.

15. The circuit of Claim 14, wherein the effective supply voltage enables at least part of a reduction in a propagation delay associated with the relatively smaller supply voltage.

16. The circuit of Claim 11, wherein the first voltage operates as a ramp and the second voltage operates as a relatively different ramp.

17. A circuit for reducing propagation delay, comprising:

a means for a logic circuit that includes a p-type transistor and an n-type transistor, wherein a drain of the p-type transistor is coupled to a drain of the n-type transistor; and

a means for a voltage offset circuit that is arranged to provide a first voltage to a gate of the p-type transistor, and further arranged to provide a second voltage to a gate of the n-type transistor such that the second voltage is positively offset relative to the first voltage.